ABSTRACT OF THE DISCLOSURE

The present invention relates to a method for controlling and for refreshing memory cells in an electrically erasable and programmable memory comprising a memory array organized in sectors, each sector comprising memory cells linked to bit lines and to word lines. The method comprises controlling and refreshing memory cells of pages of the memory array the address of which is indicated by a control and refresh counter comprising data forming tokens usable once. According to the present invention, a control and refresh counter is integrated into each sector of the memory and comprises memory cells linked to the bit lines of the sector. A counter of a sector is erased after reaching a maximum counting value that is chosen so that, when this maximum counting value is reached, memory cells of the counter have undergone a number of electrical stress cycles that is at the most equal to a determined number. Application to Flash memories.